

LLVM Passes

Ettore Speziale

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LLVM Passes

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What is Available Inside LLVM?

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LLVM provides passes performing basic transformations:

- variables promotion
- loops canonicalization
- · . . .

They can be used to normalize/canonicalize the input:

- transform into a form analyzable for further passes
- Input normalization is essential:
 - keep passes implementation manageable



Which Tongue does LLVM Speak? Static Single Assignment

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Ribliograp

LLVM IR is SSA-based:

every variable is statically assigned exactly once

Statically means that:

- inside each function
- for each variable %foo
- there is only one statement in the form %foo = ...

Static is different from dynamic:

a static assignment can be executed more than once



Static Single Assignment Examples

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Scalar SAXPY

```
float saxpy(float a, float x, float y) {
    return a * x + y;
}
```

Scalar LLVM SAXPY

```
define float @saxpy(float %a, float %x, float %y) {    %1 = fmul float %a, %x    %2 = fadd float %1, %y    ret float %2 }
```

Temporary %1 not reused for %2



Static Single Assignment Examples

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Conclusion:

Array SAXPY

```
void saxpy(float a, float x[4], float y[4], float z[4]) { for(unsigned i = 0; i < 4; ++i)          z[i] = a * x[i] + y[i]; }
```

Array LLVM SAXPY

```
; <label >:1
%i.0 = phi i32 [ 0, %0 ], [ %12, %11 ]
%2 = icmp ult i32 %i.0, 4
br i1 %2, label %3, label %13
; <label >:3
...
%12 = add i32 %i.0, 1
br label %1
```

One assignment for loop counter %i.0



Static Single Assignment Handling Multiple Assignments

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Max

LLVM Max – Bad

```
%1 = fcmp ogt float %a, %b
br i1 %1, label %2, label %3
; <label >:2
%5 = %a
br label %4
; <label >:3
%5 = %b
br label %4
; <label >:4
ret float %5
```

Why is it bad?



Static Single Assignment Use phi to Avoid Troubles

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The %5 variable must be statically set once

LLVM Max

```
%1 = fcmp ogt float %a, %b
br i1 %1, label %2, label %3
; <label >:2
br label %4
; <label >:3
br label %4
; <label >:4
%5 = phi float [ %a, %2 ], [ %b, %3 ]
ret float %5
```

The phi instructions is a conditional move:

- it takes (variable_i, label_i) pairs
- if coming from predecessor identified by *label*_i, return *variable*;



Static Single Assignment Definition and Uses

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Each SSA variable is set only once:

variable definition

Each SSA variable can be used by multiple instructions:

variable uses

Algorithms and technical language abuse of these terms:

Let %foo be a variable. If %foo definition has not side-effects, and no uses, dead-code elimination can be efficiently performed by erasing %foo definition from the CFG.



Static Single Assignment Rationale

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Old compilers are not SSA-based:

- putting input into SSA-form is expensive
- cost must be amortized

New compilers are SSA-based:

- SSA easier to work with
- SSA-based analysis/optimizations faster

All modern compilers are SSA-based:

exception is HotSpot Client compiler



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Canonicalize Pass Input

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We will see the following passes:

Useful Passes

Pass	Switch	
Variable promotion	mem2reg	
Loop simplify	loop-simplify	
Loop-closed SSA	lcssa	
Induction variable simplification	indvars	

They are normalization passes:

put data into a canonical form



Variable Promotion

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One of the most difficult things in compiler is:

considering memory accesses

Plain SAXPY

```
define float @saxpy(float %a, float %x, float %y) {
  %1 = alloca float, align 4
  %2 = alloca float, align 4
  %3 = alloca float, align 4
  store float %a, float* %1, align 4
  store float %x, float* %2, align 4
  store float float* %1, align 4
  %4 = load float* %1, align 4
  %5 = load float* %2, align 4
  %6 = fmul float %4, %5
  %7 = load float* %3, align 4
  %8 = fadd float %6, %7
  ret float %8
}
```



Variable Promotion Simplifying Representation

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In the SAXPY kernel some alloca are generated:

■ represent local variables ¹

They are generated due to compiler conservative approach:

 maybe some instruction can take the addresses of such variables, hence a memory location is needed

Complex representations makes hard performing further actions:

- suppose you want to compute a * x + y using only one instruction ²
- hard to detect due to load and store



¹Arguments are local variables

²FMA4



Variable Promotion Using Memory Only When Necessary

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To limit the number of instruction accessing memory:

- we need to eliminate load and store
- achieved by promoting variables from memory to registers

Inside LLVM SSA-based representation:

```
memory Stack allocations – e.g \%1 = alloca \text{ float}, align 4 register SSA variables – e.g. \%a
```

The mem2reg pass focus on:

eliminating alloca with only load and store uses

Also available as utility:

■ IIvm :: PromoteMemToReg



Variable Promotion Example

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Conclusion:

Promoting alloca

%1 = %a

%2 = %x

%3 = %y

%4 = %1

%5 = %2

%6 = fmul %4, %5

%7 = %3

%8 =fadd %6. %7

ret %8

After Copy-propagation

%1 = fmul %a, %x %2 = fadd %1, %y ret %2

Starting Point

%1 = alloca float %2 = alloca float %3 = alloca float

store %a, %1 store %x, %2

store %y, %3 %4 = load %1

%5 = load %2

%6 = fmul %4, %5 %7 = load %3

%7 = 10ad %5%8 = fadd %6, %7

ret %8

Copy propagation performed transparently by the compiler



Loops

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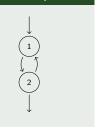
do-while Loops

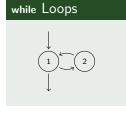
..

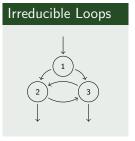
Normalization Passes

Analysis Passes

Conclusion







Focus is on one kind of loops:

■ natural loops



Natural Loops

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A natural loop:

- has only one entry node header
- there is a back edge that enter the loop header

Under this definition:

- the irreducible loop is not a natural loop
- since LLVM consider only natural loops, the irreducible loop is not recognize as a loop



Loop Terminology

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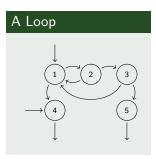
Analysis

Conclusions

n....

Loops defined starting from back-edges:

back-edge edge entering loop header: (3,1)



header loop entry node: 1
body nodes that can reach
back-edge source
node - 3 - without
passing from
back-edge target
node - 1 - plus
back-edge target
node: {1,2,3}

exiting nodes with a successor outside the loop: $\{1,3\}$ exit nodes with a predecessor inside the loop: $\{4,5\}$



Loop Simplify

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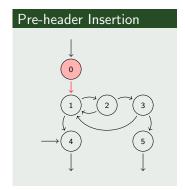
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Natural loops allows to identify loops:

■ some features are not analysis/optimization friendly

The loop-simplify pass normalize natural loops:

pre-header the only
predecessor of
header node
latch the starting node
of the only
back-edge
exit-block ensures exits
dominated by
loop header





Loop Simplify Example

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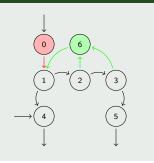
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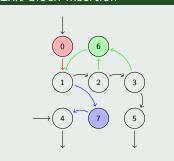
Analysis

Conclusion

Latch Insertion



Exit-block Insertion



- pre-header always executed before entering the loop
- latch always executed before starting a new iteration
- exit-blocks always executed after exiting the loop



Loop-closed SSA

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Loop representation can be further normalized:

- loop-simplify normalize the shape of the loop
- nothing is said about loop definitions

Keeping SSA form is expensive with loops:

- 1cssa insert phi instruction at loop boundaries for variables defined inside the loop body and used outside
- this guarantee isolation between optimization performed inside and outside the loop
- faster keeping IR into SSA form propagation of code changes outside the loop blocked by phi instructions



Loop-closed SSA Example

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Conclusion

```
Linear Search
```

```
unsigned search(float *x, unsigned n, float y) {
  unsigned i, j = 0;
  for(i = 0; i != n; ++i)
    if(x[i] == y)
        j = i;
  return j;
}
```

The example is trivial:

- think about having large loop bodies
- transformation becomes useful



Loop-closed SSA Example

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Conclusion:

Before LCSSA

```
\%i.0 = phi i32 [0, \%0], [\%10, \%9]
 \%j.0 = phi i32 [ 0, \%0 ], [ \%j.1, \%9 ]
 \%2 = icmp ne i32 \%i.0, \%n
 br i1 %2, label %3, label %11
: < label >:3
 br i1 %6, label %7, label %8
: < label >:7
 br label %8
: < label >:8
 \%j.1 = phi i32 [ %i.0, %7 ], [ %j.0, %3 ]
 br label %9
: < label >:9
 \%10 = add i32 \%i.0.1
 br label %1
; < label >:11
  ret i32 %j.0
```



Loop-closed SSA Example

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```
After LCSSA
```

```
\%i.0 = phi i32 [0, \%0], [\%10, \%9]
 \%j.0 = phi i32 [ 0, \%0 ], [ \%j.1, \%9 ]
 %2 = icmp ne i32 \%i.0, %n
 br i1 %2, label %3, label %11
: < label >:3
  br i1 %6, label %7, label %8
; < label >:7
  br label %8
: < label >:8
 \%j.1 = phi i32 [ %i.0, %7 ], [ %j.0, %3 ]
  br label %9
: < label >:9
 \%10 = add i32 \%i.0.1
 br label %1
: < label >:11
 \%j.0.lcssa = phi i32 [ \%j.0, \%1 ]
  ret i32 %j.0. lcssa
```



Induction Variables

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Some loop variables are *special*:

■ e.g. counters

Generalization lead to induction variables:

foo is a loop induction variable if its successive values form an arithmetic progression:

$$foo = bar * baz + biz$$

where bar, biz are loop-invariant 3 , and baz is an induction variable

■ foo is a canonical induction variable if it is always incremented by a constant amount:

$$foo = foo + biz$$

where biz is loop-invariant



³Constants inside the loop



Induction Variable Simplification

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Conclusion:

....

Canonical induction variables are used to drive loop execution:

given a loop, the indvars pass tries to find its canonical induction variable

With respect to theory, LLVM canonical induction variable is:

- initialized to 0
- incremented by 1 at each loop iteration



Normalization Wrap-up

LIVM Passes

Normalization Passes

Normalization passes running order:

- 11 mem2reg: limit use of memory, increasing the effectiveness of subsequent passes
- 2 loop-simplify: canonicalize loop shape, lower burden of writing passes
- 3 lcssa: keep effects of subsequent loop optimizations local, limiting overhead of maintaining SSA form
- 4 indvars: normalize induction variables, highlighting the canonical induction variable

Other normalization passes available:

■ try running opt -help



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Checking Input Properties

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Analysis basically allows:

inspecting input

Keeping analysis information is expensive:

- tuned algorithms updates analysis information when an optimization invalidates them
- incrementally updating analysis is cheaper than recomputing them

Many LLVM analysis supports incremental updates:

- this is an optimization
- forget this feature for the home-work
- focus on information provided by analysis



Useful Analysis

LLVM Passes

Analysis Passes

We will see the following passes:

Analysis

Pass	Switch	Transitive
Control flow graph	none	No
Dominator tree	domtree	No
Post-dominator tree	postdomtree	No
Loop information	loops	Yes
Scalar evolution	scalar-evolution	Yes
Alias analysis	special	Yes
Memory dependence	memdep	Yes

Requiring analysis by transitivity:

Yes IIvm :: AnalysisUsage :: addRequiredTransitive<T>()

NO IIvm :: AnalysisUsage :: addRequired<T>()





Control Flow Graph

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Conclusions

The Control Flow Graph is implicitly maintained by LLVM:

no specific pass to build it

Recap:

- CFG for a function is a set of basic blocks
- a basic block is a set of instructions

Functions and basic blocks acts like containers:

- STL-like accessors: front(), back(), size(), . . .
- STL-like iterators: begin(), end()

Each contained element is aware of its container:

■ getParent()



Control Flow Graph Walking

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Every CFG has an entry basic block:

- the first executed basic block
- it is the root/source of the graph
- get it with Ilvm::Function::getEntryBlock()

More than one exit blocks can be generated:

- their terminator instructions are rets
- they are the leaves/sinks of the graph
- use Ilvm::BasicBlock::getTerminator() to get the terminator . . .
- ... then check its class



Side Note Casting Framework

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For performance reasons, a custom casting framework is used:

you cannot use static_cast and dynamic_cast with types/classes provided by LLVM

LLVM Casting Functions

Function
X * Ilvm :: cast < X > (Y *)
$X * Ilvm :: dyn_cast < X > (Y *)$
bool IIvm :: isa $<$ X $>(Y *)$

Example:

■ is BB a sink?

Ilvm :: isa < Ilvm:: ReturnInst > (BB.getTerminator())



Control Flow Graph Basic Blocks

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Every basic block BB has one or more:

predecessors from pred_begin(BB) to pred_end(BB)

SUCCESSORS from succ_begin(BB) to succ_end(BB)

Convenience accessors directly available in Ilvm:: BasicBlock:

■ e.g. IIvm :: BasicBlock :: getUniquePredecessor()

Other convenience member functions:

moving a basic block:

Ilvm :: BasicBlock :: moveBefore(Ilvm::BasicBlock *) Or

Ilvm :: BasicBlock :: moveAfter(Ilvm :: BasicBlock *)

split a basic block:

Ilvm :: BasicBlock :: splitBasicBlock (Ilvm :: BasicBlock :: iterator)

. . . .



Control Flow Graph Instructions

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The IIvm:: Instruction class define common operations:

■ e.g. getting an operand: Ilvm:: Instruction::getOperand(unsigned)

Subclasses provide specialized accessors:

The value produced by the instruction is the instruction itself:

Example

Consider:

$$\%6 = load i32* \%1, align 4$$

the load is described by an instance of Ilvm::LoadInst. That instance also models the %6 variable



Instructions Creating New Instructions

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Instructions built using:

- constructors e.g. Ilvm :: LoadInst :: LoadInst (...)
- factory methods e.g. Ilvm :: GetElementPtrInst :: Create (...)

Interface is not homogeneous:

- some instructions support both methods
- others support only one

At build-time, instructions can be:

- appended to a basic block
- inserted after/before a given instruction

Insertion point usually specified as builder last argument



Side Note Definitions and Uses

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Ribliogran

LLVM class hierarchy is built around two simple concepts:

value something that can be used: Ilvm::Value

user something that can use: Ilvm::User

A value is a definition:

■ Ilvm::Value::use_begin(), Ilvm::Value::use_end() to visit uses

An user access definitions:

■ Ilvm::User::op_begin(), Ilvm::User::op_end() to visit used values

Functions:

Instructions:

■ used by call sites

define an SSA value

uses formal parameters

uses operands



Side Note Value Typing

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D'I-I' - I

Every Ilvm :: Value is typed:

■ use Ilvm::Value::getType() to get the type

Since every instructions is/define a value:

instructions are typed

Example

Consider:

$$\%6 =$$
load i32* $\%1$, align 4

the %6 variable actually is the instruction itself. Its type is the type of load return value, i32



Dominance Trees

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D:h::-----

Dominance trees answer to control-related queries:

- is this basic block executed before that?
- IIvm :: DominatorTree

- is this basic block executed after that?
- IIvm :: PostDominatorTree

The two trees interface is similar:

- bool dominates(X *, X *)
- **bool** properlyDominates(X *, X *)

Where X is an Ilvm:: BasicBlock or an Ilvm:: Instruction

Using opt is possible printing them:

- -view-dom, -dot-dom
- -view-postdom, -dot-postdom





Loop Information

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Conclusion:

Loop information are represented using two classes:

■ Ilvm::LoopInfo analysis detects natural loops

■ Ilvm::Loop represents a single loop

Using Ilvm::LoopInfo it is possible:

navigate through top-level loops:

Ilvm :: LoopInfo :: begin(), Ilvm :: LoopInfo :: end()

get the loop for a given basic block:

Ilvm :: LoopInfo :: operator [](Ilvm :: BasicBlock *)



Loop Information Nesting Tree

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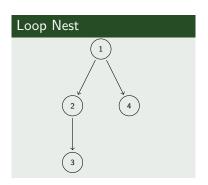
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Loops are represented in a nesting tree:

```
Source
while(i < 10) {
   while(j < 10)
      while(k < 10)
      ...
   while(h < 10)
      ...
}</pre>
```



Nest navigation:

- children loops: Ilvm::Loop::begin(), Ilvm::Loop::end()
- parent loop: Ilvm :: Loop::getParentLoop()



Loop Information Query Loops

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Accessors for relevant nodes also available:

pre-header IIvm :: Loop:getLoopPreheader()

header IIvm :: Loop::getHeader()

latch IIvm :: Loop::getLoopLatch()

exiting Ilvm::Loop::getLoopExiting(),

Ilym ... I con... got Eviting Placks /

Ilvm :: Loop:: getExitingBlocks (...)

exit IIvm :: Loop::getExitBlock()

Ilvm :: Loop::getExitBlocks (...)

Loop basic blocks accessible via:

iterators Ilvm::Loop::block_begin(),

IIvm :: Loop::block_end()

Vector std::vector<llvm::BasicBlock *> &Ilvm::Loop::getBlocks()



Loop Information Query Loop Instructions

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Conclusion:

Other IIvm::Loop accessors:

canonical induction variable:

Ilvm :: Loop:: getCanonicalInductionVariable ()

trip count:

IIvm :: Loop::getTripCount()

The trip count is a Ilvm::Value:

- indicates the number of iterations composing the loop
- not always possible computing it



Scalar Evolution

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The SCalar EVolution framework:

- represents scalar expressions
- supports recursive updates
- lower burden of explicitly handling expressions composition
- is designed to support general induction variables

Example

```
; <label>:1
%i.0 = phi [ 0, %0 ], [ %11, %2 ]
%exitcond = icmp ne %i.0, 10
br %exitcond, label %2, label %3
; <label>:2
%11 = add nsw %i.0, 1
br label %1
```

SCEV for %i.0:

- initial value 0
- incremented
- by 1 at each iteration
- final value 10



Scalar Evolution Example

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D:h::-----

Source

```
void foo() {
  int bar[10][20];

for(int i = 0; i < 10; ++i)
  for(int j = 0; j < 20; ++j)
    bar[i][j] = 0;
}</pre>
```

SCEV $\{A,B,C\}<\%D>:$

- A initial
- B operator
- C operand
- D defining BB

Induction Variables

```
%i.0 = phi i32 [ 0, %0 ], [ %11, %10 ] 

\longrightarrow {0,+,1}<nuw>nsw>%1> Exits: 10 

%j.0 = phi i32 [ 0, %2 ], [ %8, %7 ] 

\longrightarrow {0,+,1}<nuw>nsw>%3> Exits: 20
```



Scalar Evolution More than Induction Variables

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The scalar evolution framework manages any scalar expression:

Pointer SCEVs

```
%5 = getelementptr %bar, i32 0, i32 %i.0

--> {%bar,+,80} < nsw >< %1>

Exits: {%bar,+,80} < nsw >< %1>

%6 = getelementptr %5, i32 0, i32 %j.0

--> {{%bar,+,80} < nsw >< %1>,+,4} < nsw >< %3>

Exits: {(80 + %bar),+,80} < nw >< %1>
```

SCEV is an analysis used for common optimizations:

- induction variable substitution
- strength reduction
-



Scalar Evolution SCEVs Design

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SCEVs are modeled by the IIvm::SCEV class:

- a subclass for each kind of SCEV: e.g. Ilvm::SCEVAddExpr
- instantiation disabled

A SCEV actually is a tree of SCEVs:

$$\blacksquare$$
 {(80 + %bar),+,80} = {%1,+,80}, %1 = 80 + %bar

Tree leaves:

constant IIvm::SCEVConstant: e.g. 80

unknown 4 Ilvm::SCEVUnknown: e.g. %bar

SCEV tree explorable through the visitor pattern:

■ Ilvm :: SCEVVisitor

⁴Not further splittable



Scalar Evolution Analysis Interface

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The IIvm :: ScalarEvolution class:

- analyzes SCEVs for a IIvm :: Function
- builds SCEVs for values:

Ilvm :: ScalarEvolution :: getSCEV(Ilvm::Value *)

creates new SCEVs:

```
\label{lvm::ScalarEvolution::getConstant(llvm::ConstantInt *)} \\ Ilvm::ScalarEvolution::getAddExpr(Ilvm::SCEV *, Ilvm::SCEV *) \\ \\
```

. . .

gets important SCEVs:

```
Ilvm :: ScalarEvolution :: getBackedgeTakenCount(Ilvm::Loop *)
```

Ilvm :: ScalarEvolution :: getPointerBase(Ilvm :: SCEV *)

. . .



Alias Analysis

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Let X be an instruction accessing a memory location:

is there another instruction accessing the same location?

Alias analysis tries to answer the question:

application memory operation scheduling problem often fails

Different algorithms for alias analysis:

- common interface Ilvm:: AliasAnalysis for all algorithms
- by default, basic alias analyzer basicaa is used

Requiring Alias Analysis

AU.addRequiredTransitive < IIvm :: AliasAnalysis > ();



Alias Analysis Memory Representation

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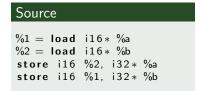
Introduction

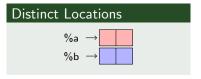
Normalization Passes

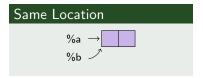
Analysis Passes

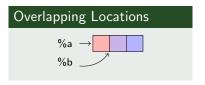
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Basic building block is Ilvm :: AliasAnalysis :: Location:

- address: e.g. %a
- size: e.g. 2 bytes



Alias Analyzer Basic Interface

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Given two locations X, Y, the alias analyzer classifies them:

- Ilvm :: AliasAnalyzer :: NoAlias: X and Y are different memory locations
- Ilvm:: AliasAnalyzer:: MustAlias: X and Y are equal i.e. they points to the same address
- Ilvm:: AliasAnalyzer:: PartialAlias: X and Y partially overlap i.e. they points to different addresses, but the pointed memory areas partially overlap
- Ilvm:: AliasAnalyzer:: MayAlias: unable to compute aliasing information i.e. X and Y can be different locations, or X can be a complete/partial alias of Y

Queries performed using:

■ Ilvm :: AliasAnalyzer :: alias (X, Y)



Alias Analyzer Mid-level Interface

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Basic alias analyzer interface is low-level – we would like expressing queries about a single pointer X:

- how referenced memory location is accessed?
- which other instructions reference the same location?

What we need is a set, to classify memory locations:

- Construct a Ilvm:: AliasSetTracker starting from a Ilvm:: AliasAnalyer *
- it builds IIvm :: AliasSetS

For a given location X, a llvm :: AliasSet:

 \blacksquare contains all locations aliasing with X



Alias Analyzer Alias Set Memory Accesses

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Each alias set references the memory:

- Ilvm :: AliasSet :: NoModRef: no memory reference i.e. the set is empty
- Ilvm:: AliasSet:: Mod: memory accessed in write-mode e.g. a store is inside the set
- Ilvm:: AliasSet:: Ref: memory accessed in read-mode e.g. a load is inside the set
- Ilvm:: AliasSet:: ModRef: memory accessed in read-write mode
 e.g. a load and a store inside the set



Alias Analyzer Mid-level Interface

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Entry point is IIvm:: AliasSetTracker:: getAliasSetForPointer (...):

- Ilvm::Value *: location address
- uint64_t: location size
- Ilvm:: MDNode *: used for type-based alias analysis ⁵
- bool *: whether a new Ilvm:: AliasSet has been created to hold the location location does not alias up to now

Having the Ilvm :: AliasSet:

- STL container-like interface: size(), begin(), end(), . . .
- check reference type: Ilvm :: AliasSet :: isRef(), . . .
- check aliasing type: Ilvm:: AliasSet::isMustAlias(), ...

⁵set to NULL



Memory Dependence Analysis Alias Analyzer High-level Interface

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The IIvm::MemoryDependenceAnalysis wraps alias analysis to answer queries in the following form:

■ let %foo be an instruction accessing memory. Which preceding instructions does %foo depends on?

Reads:

stores writing memory locations aliases with the one references by %foo

Writes:

loads reading memory locations aliased with the one referenced by %foo



Memory Dependence Analysis

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D'L1'

Let %foo be a Ilvm:: Instruction accessing memory:

- Call IIvm :: MemoryDependenceAnalysis::getDependency(...)
- you get a llvm :: MemDepResult

Dependencies are classified:

- Ilvm::MemDepResult::isClobber(): an instruction clobbering i.e. potentially modifying location referenced by %foo has been found
- Ilvm::MemDepResult::isDef(): an instruction defining e.g. writing the exact location referenced by %foo has been found
- Ilvm::MemDepResult::isNonLocal(): no dependency found on %foo basic block
- Ilvm::MemDepResult::isNonFuncLocal(): no dependency found on %foo function





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Inside LLVM there a lot of passes:

normalization put program into a canonical form analysis get info about program

Please remember that

- a good compiler writer re-uses code
- check LLVM sources before re-implementing a pass



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